ABSTRACT:

The present invention relates to a signal processing device and method of supplying a signal processing result to a plurality of registers arranged in different register files, wherein a plurality of different register files are selected based on a corresponding indication in said instruction word, and the register address is supplied to said selected register files. Thereby, result values can be broadcasted to multiple registers in a single processor cycle, while a copy operation between different register files is eliminated. Broadcasting is thus implemented via overlapping register address spaces, since physical registers having the same logical register address are provided in different register files.

(Fig. 1)